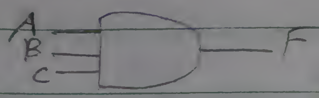
Digital ~~Design~~ Systems

<u>Part 2</u> Logic Design — د. أماني

<u>part 1</u> VHDL — د. محمود المنوفي

AND



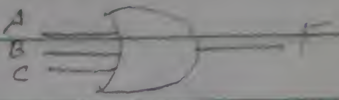
1 if all input = 1

$F = A.B.C. ..$

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

2^n

OR



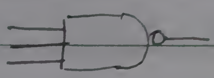
$F = A + B + C$

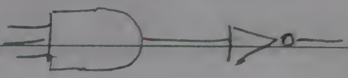
1 if any input = 1

Inverter (NOT)

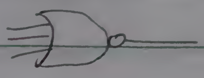
A	$\bar{A}$
0	1
1	0

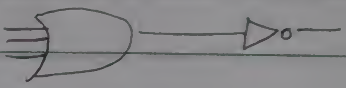
NAND



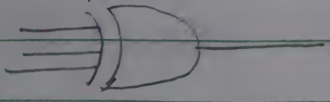


NOR





XOR

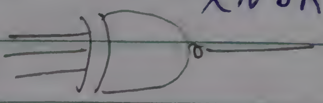


1 if no. 1 input odd

x	y	F
0	0	0
0	1	1
1	0	1
1	1	0

$F = x \oplus y$

XNOR



1 if no. 1 input even

x	y	F
0	0	1
0	1	0
1	0	0
1	1	1

$F = x \odot y$

Karnaf Map

BC \ A	0	1
00	0	1
01	1	0
11	1	0
10	0	1

$F = A'C + AC'$

Sum of product

Sum of min term (تبسيط)

$F' = AC + A'C'$

$F = (A' + C')(A + C)$

product of sum

product of max term (غير مبسط)

$F = C' + \bar{A}\bar{B} + \bar{A}\bar{D}$

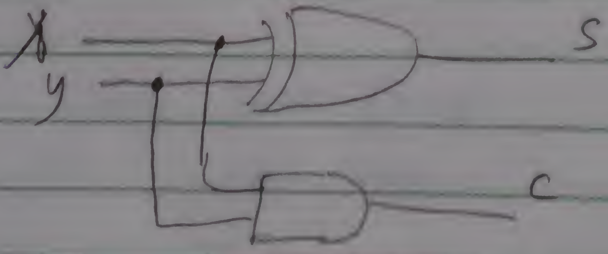
CD \ AB	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1			
10	1	1		

C' , $\bar{A}B'$, $A'D'$

Adder

Half Adder

x	y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

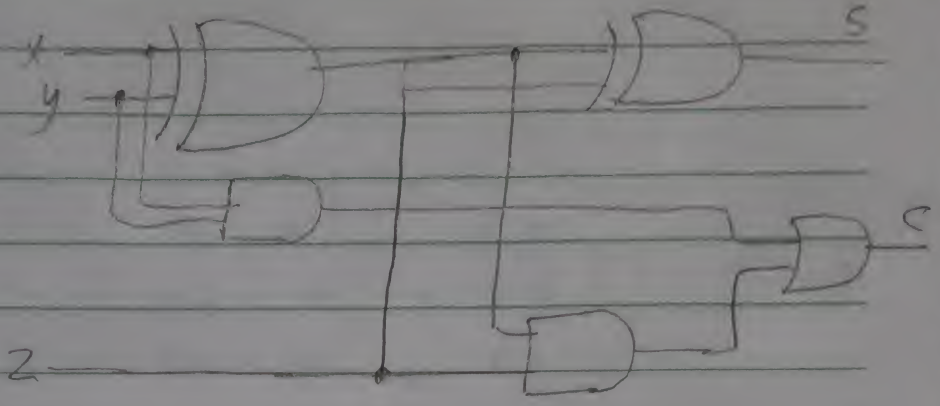


$S = x \oplus y$

$C = xy$

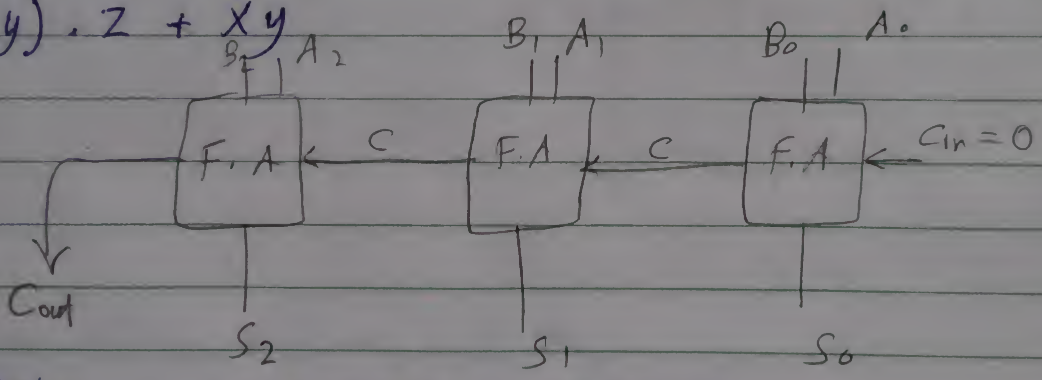
Full Adder

X	y	z	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



$S = X \oplus y \oplus Z$

$C = (X \oplus y) \cdot Z + Xy$



<u>Carry Delay</u> = 2n + 2 gate delay

Carry look Ahead

<u>Carry Delay</u> = 4 gate delay

Date :

Decoder

n Inputs $\qquad 2^n$ output

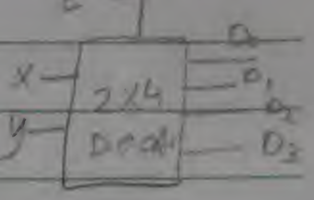
x	y	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

$D_0 = m_0 = x'y'$

$D_1 = m_1 = x'y$

$D_2 = m_2 = xy'$

$D_3 = m_3 = xy$

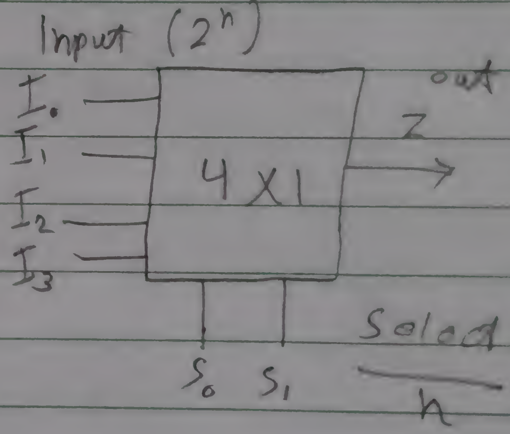


High E on E = 1

Low E on E = 0

Multiplexer Mux

S_1	S_0	Z
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



$$Z = I_0 m_0 + I_1 m_1 + I_2 m_2 + I_3 m_3$$